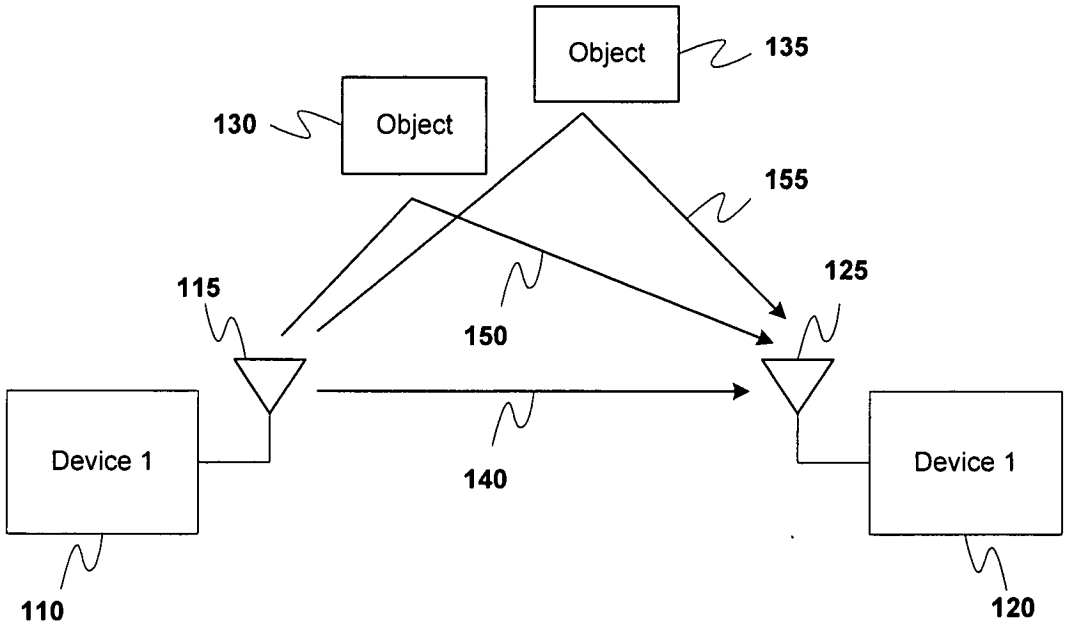
Object
135
Object
130
155
115
125
150
Device 1
140
Device 1
110
120

Fig. 1

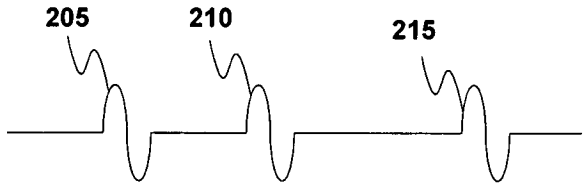

Fig. 2A

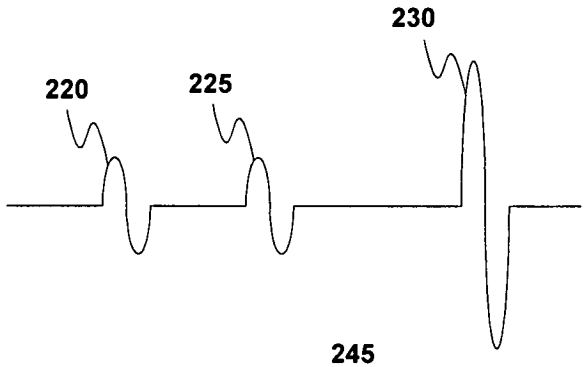

Fig. 2B

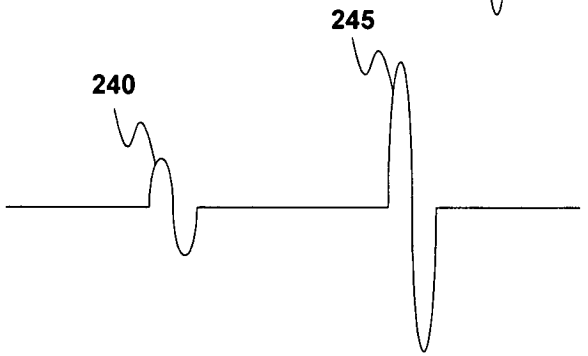

Fig. 2C

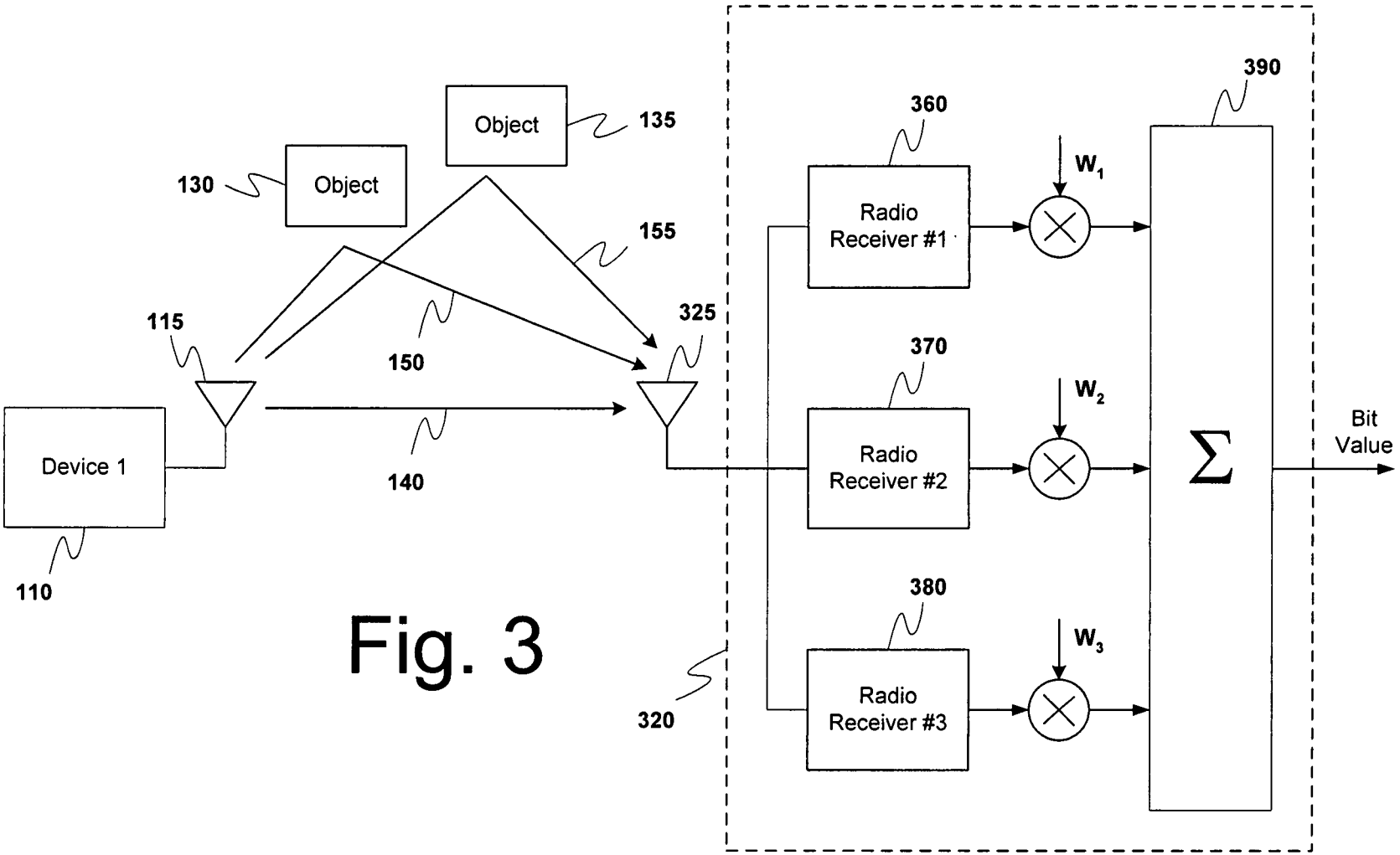
Object
135
Object
130
155
115
150
325
Device 1
140
110
360
390
Radio
Receiver #1
W1
370
Radio
Receiver #2
W2
Σ
Bit
Value
380
Radio
Receiver #3
W3
320

Fig. 3

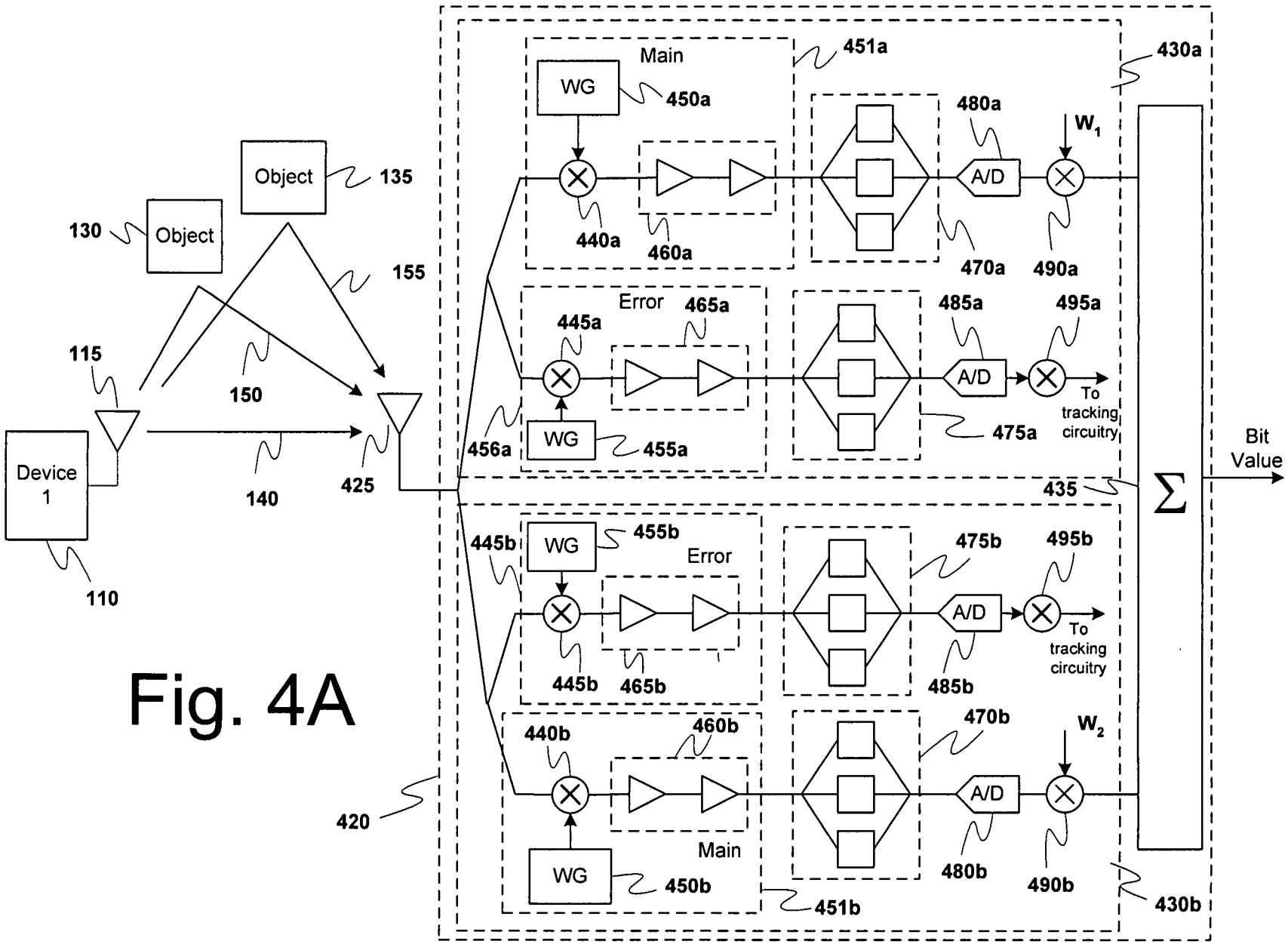
Object
135
Object
130
155
115
150
Device
1
140
425
110
420
Main
WG
450a
451a
430a
480a
W_1
A/D
440a
460a
470a
490a
Error
465a
445a
485a
495a
A/D
To
tracking
circuitry
456a
WG
455a
475a
435
Bit
Value
Σ
445b
WG
455b
Error
475b
495b
A/D
To
tracking
circuitry
445b
465b
485b
440b
460b
470b
W_2
A/D
Main
WG
450b
451b
480b
490b
430b

Fig. 4A

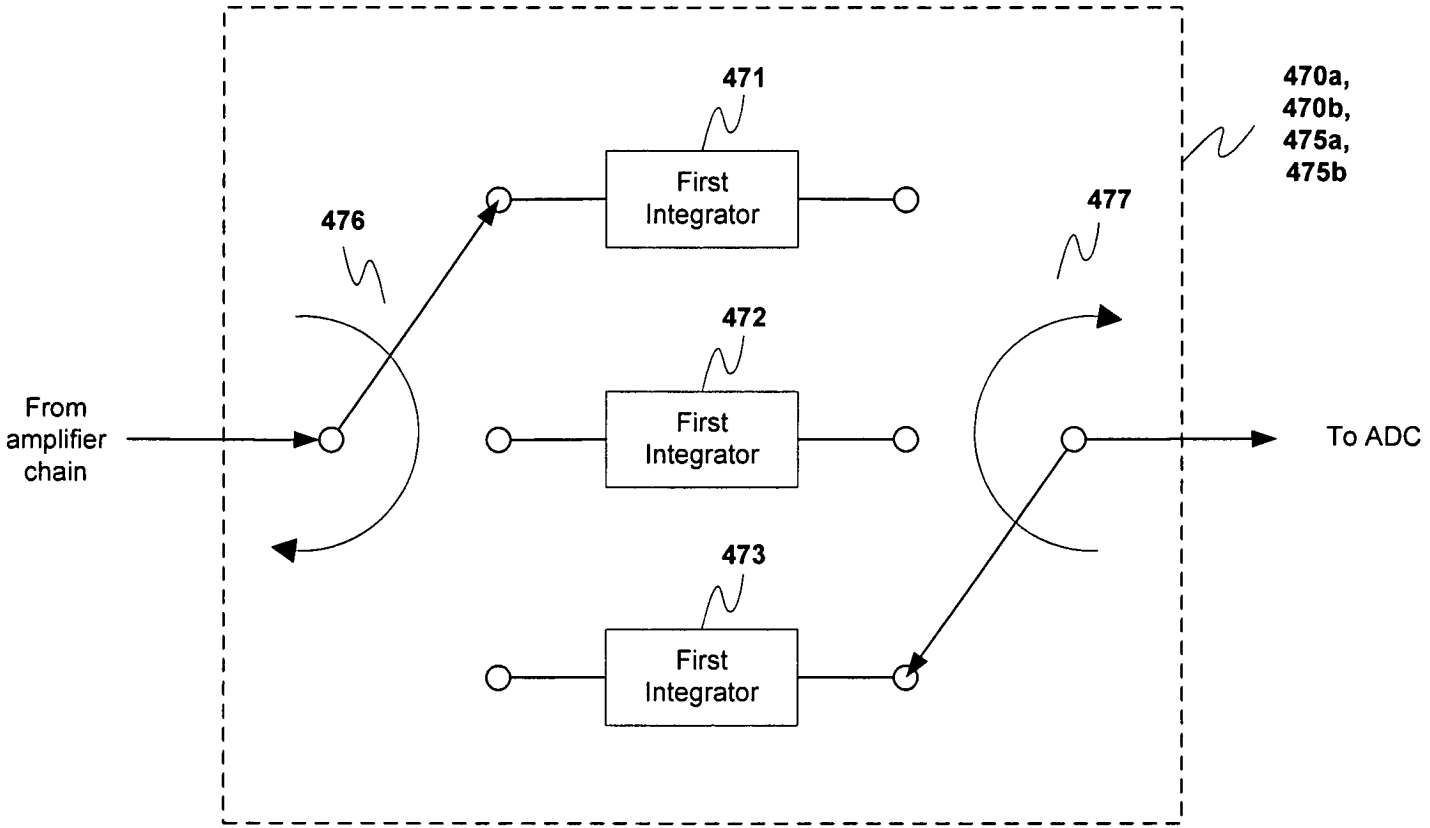
471
First Integrator
472
First Integrator
473
First Integrator
476
477
470a, 470b, 475a, 475b
From amplifier chain
To ADC

Fig. 4B

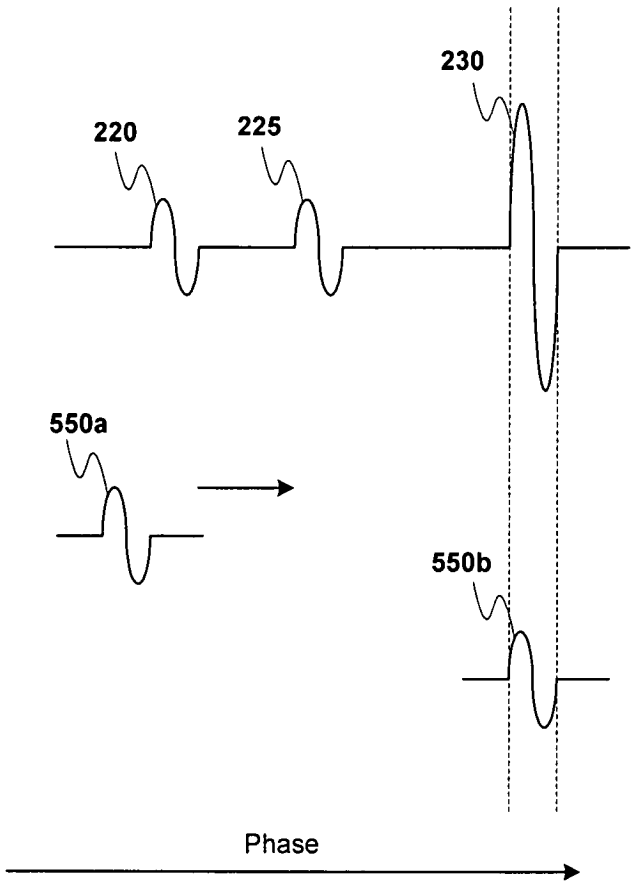

Fig. 5

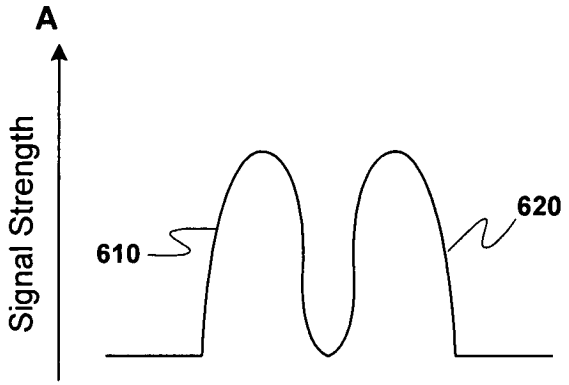

Fig. 6

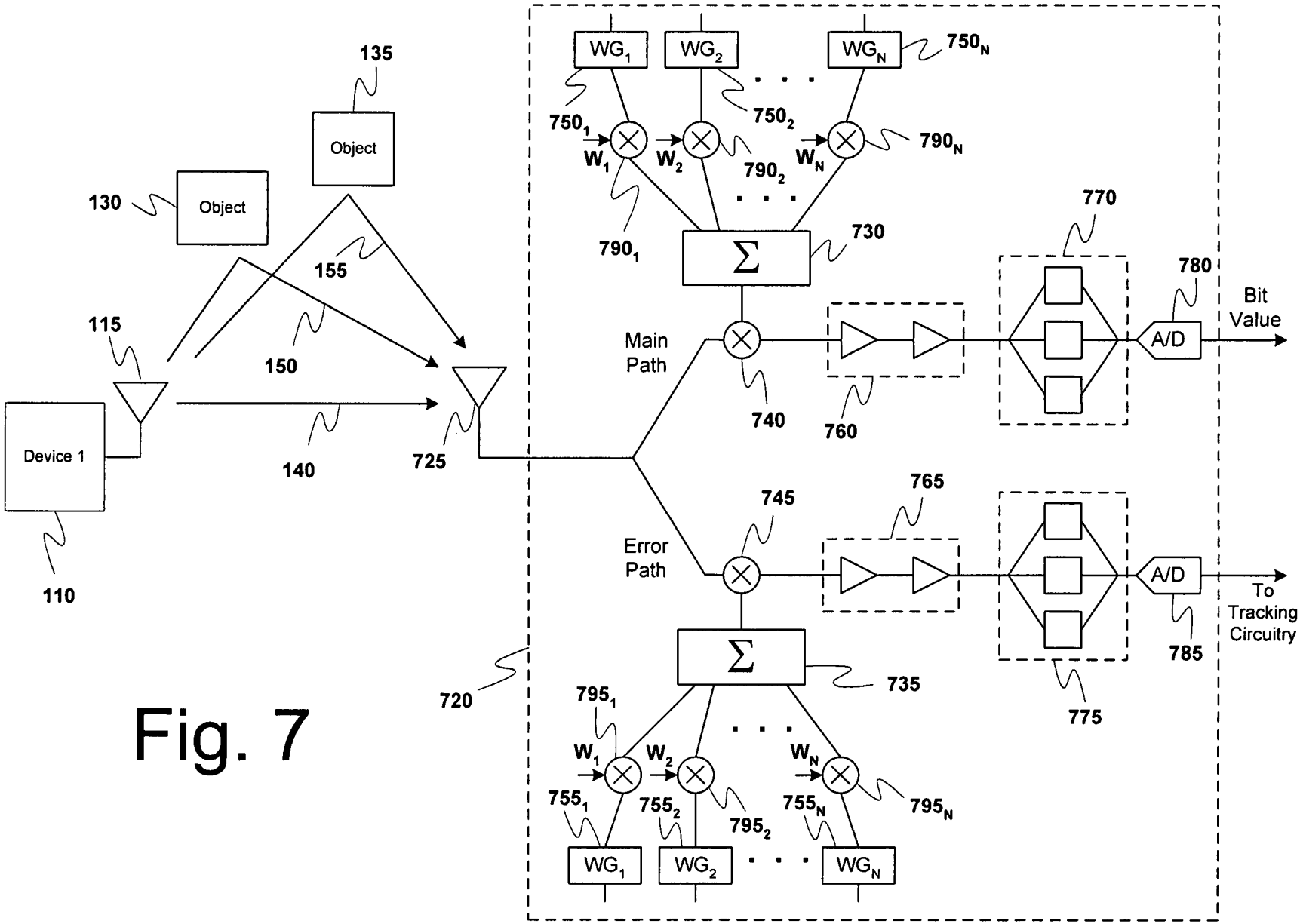
135
Object
130
Object
155
115
150
Device 1
140
110
725
720
WG1
WG2
WGN
750N
750₁
750₂
W1
W2
WN
790N
790₂
790₁
730
Σ
770
780
Bit Value
Main Path
A/D
740
760
745
765
Error Path
A/D
To Tracking Circuitry
785
775
735
795₁
795₂
795N
755₁
755₂
755N

Fig. 7

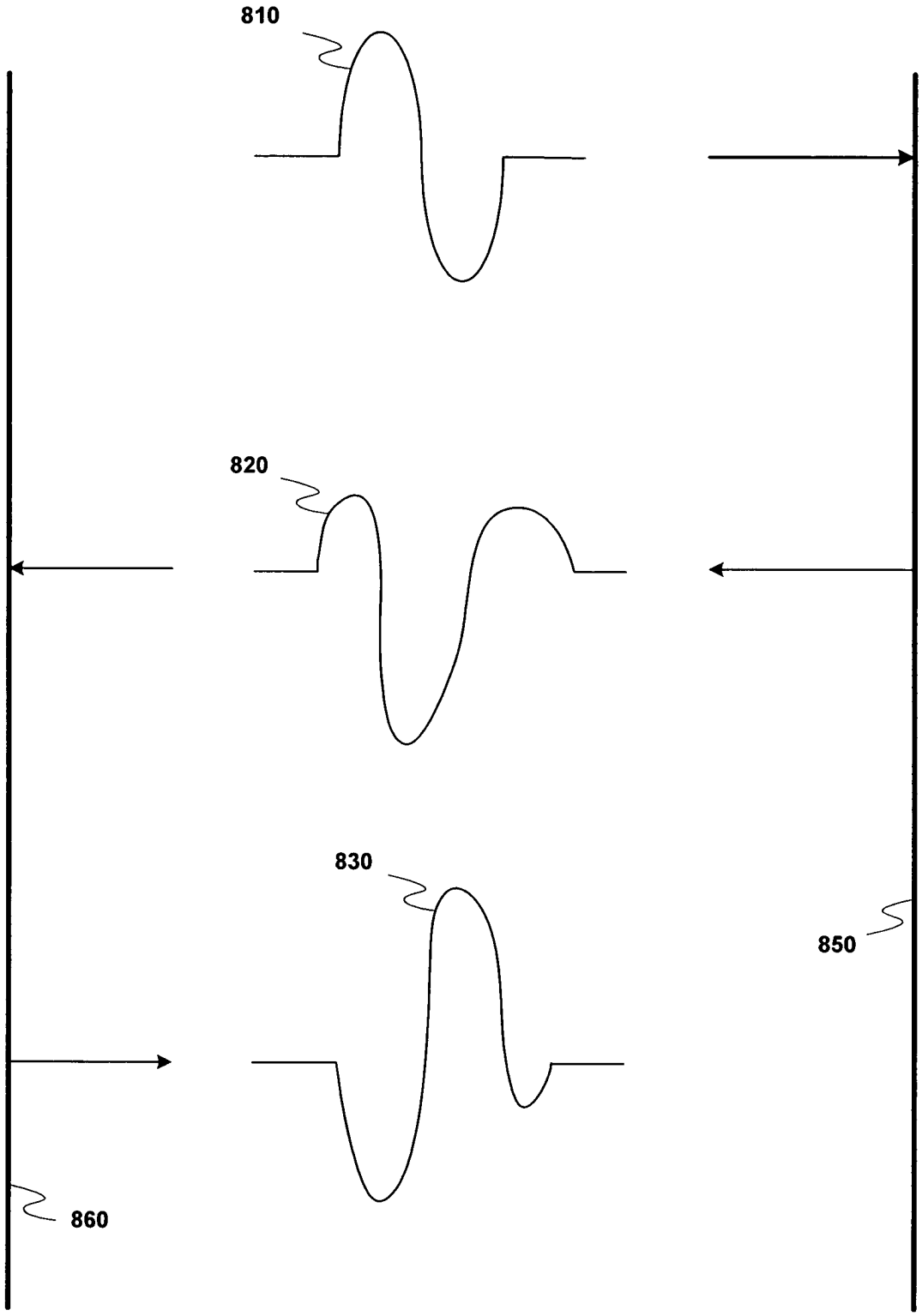

Fig. 8

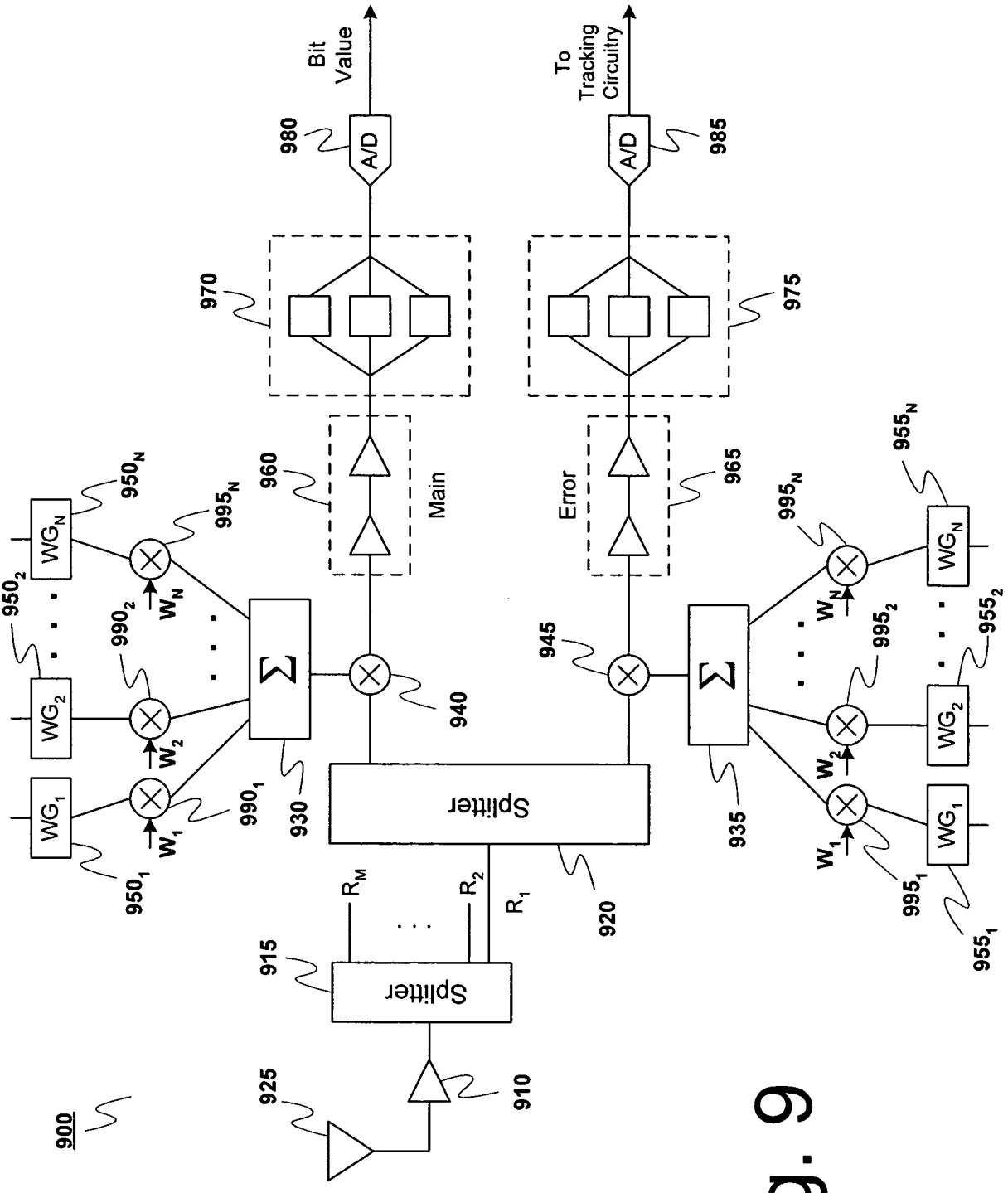
900
925
910
915
Splitter
R_M
R_2
R_1
920
Splitter
930
940
945
935
960
Main
965
Error
970
975
980
A/D
Bit Value
985
A/D
To Tracking Circuitry
WG_1
WG_2
WG_N
950_1
950_2
950_N
990_1
990_2
995_N
W_1
W_2
W_N
955_1
955_2
955_N
995_1
995_2
995_N

Fig. 9

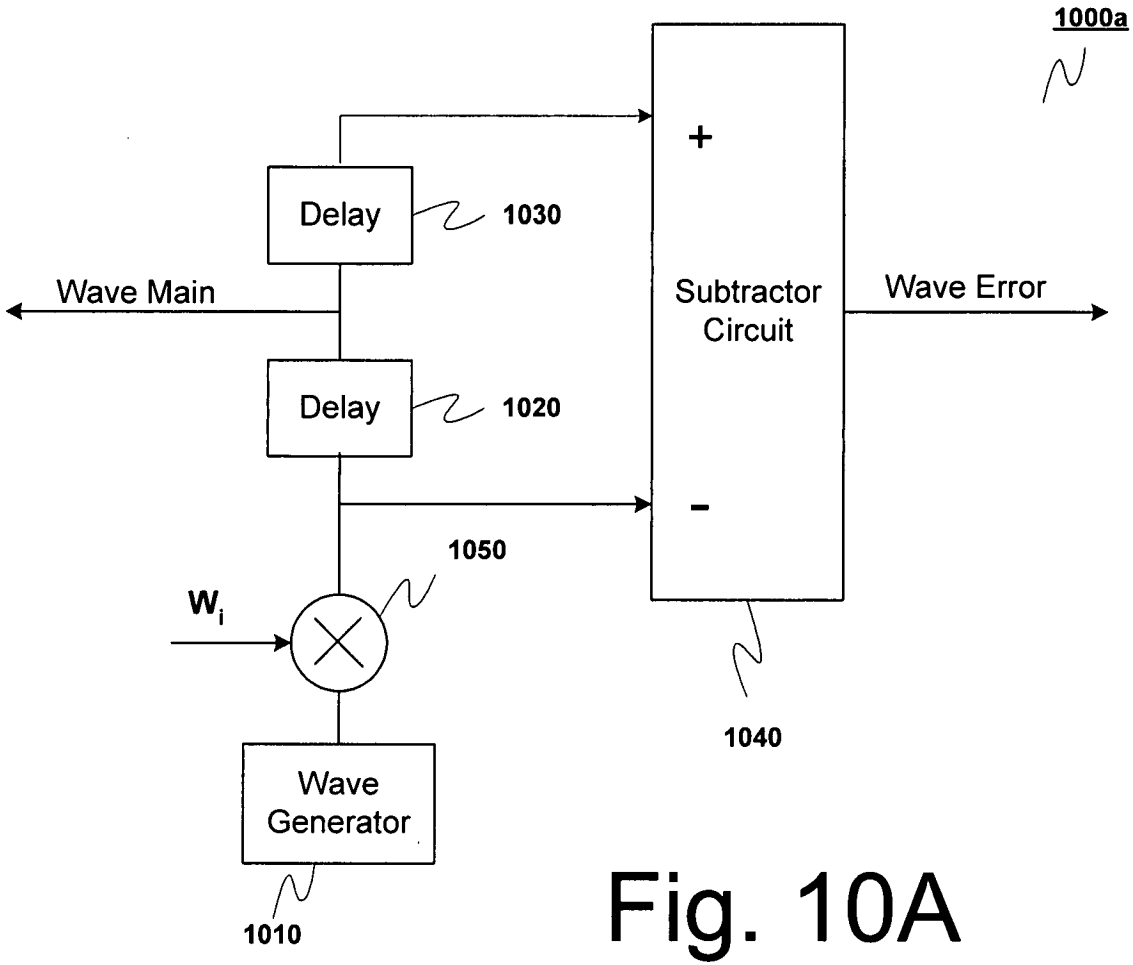
1000a
+
Delay
1030
Wave Main
Subtractor Circuit
Wave Error
Delay
1020
-
1050
W_i
1040
Wave Generator
1010

Fig. 10A

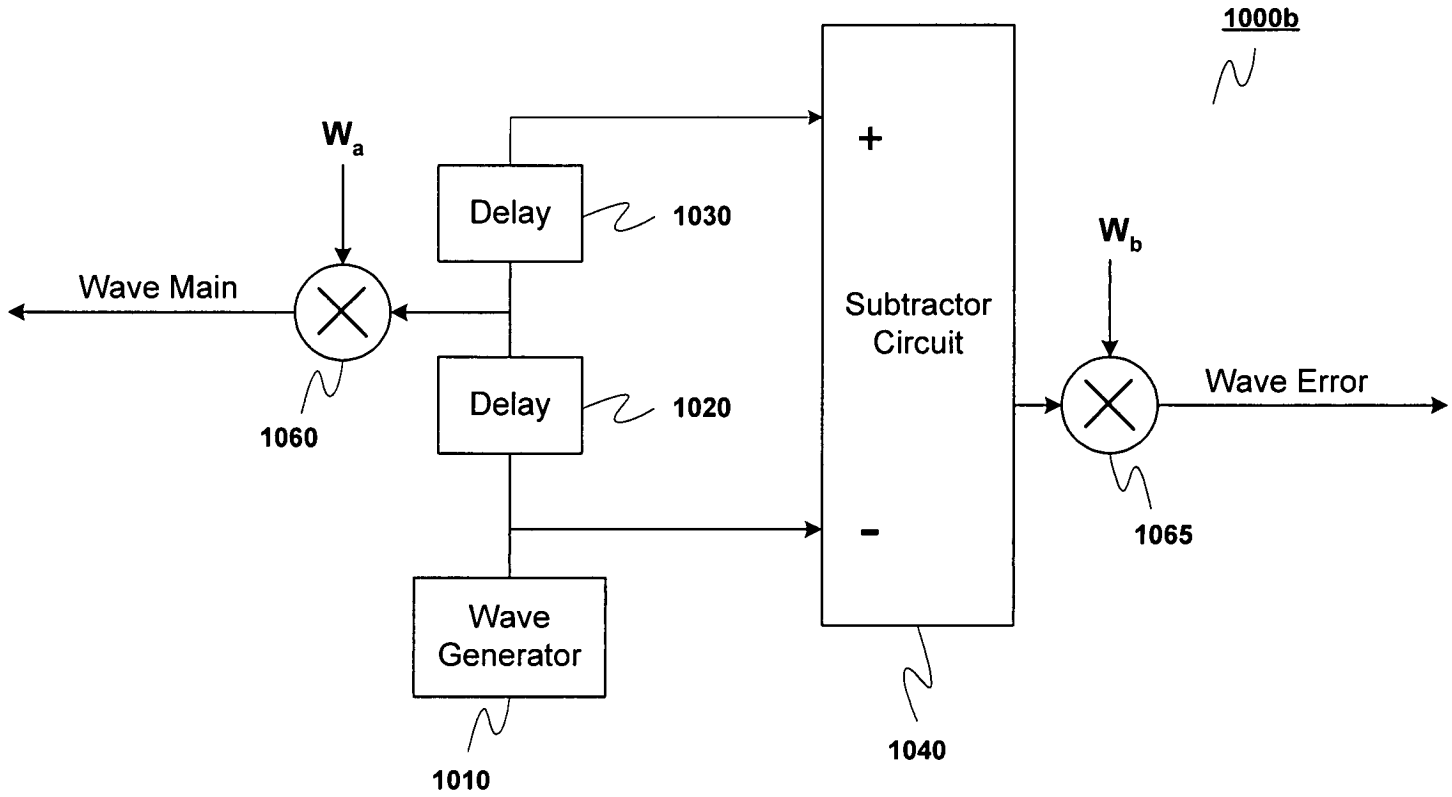
1000b
W_a
Delay
1030
Wave Main
Delay
1020
1060
Wave Generator
1010
+
Subtractor Circuit
-
1040
W_b
Wave Error
1065

Fig. 10B

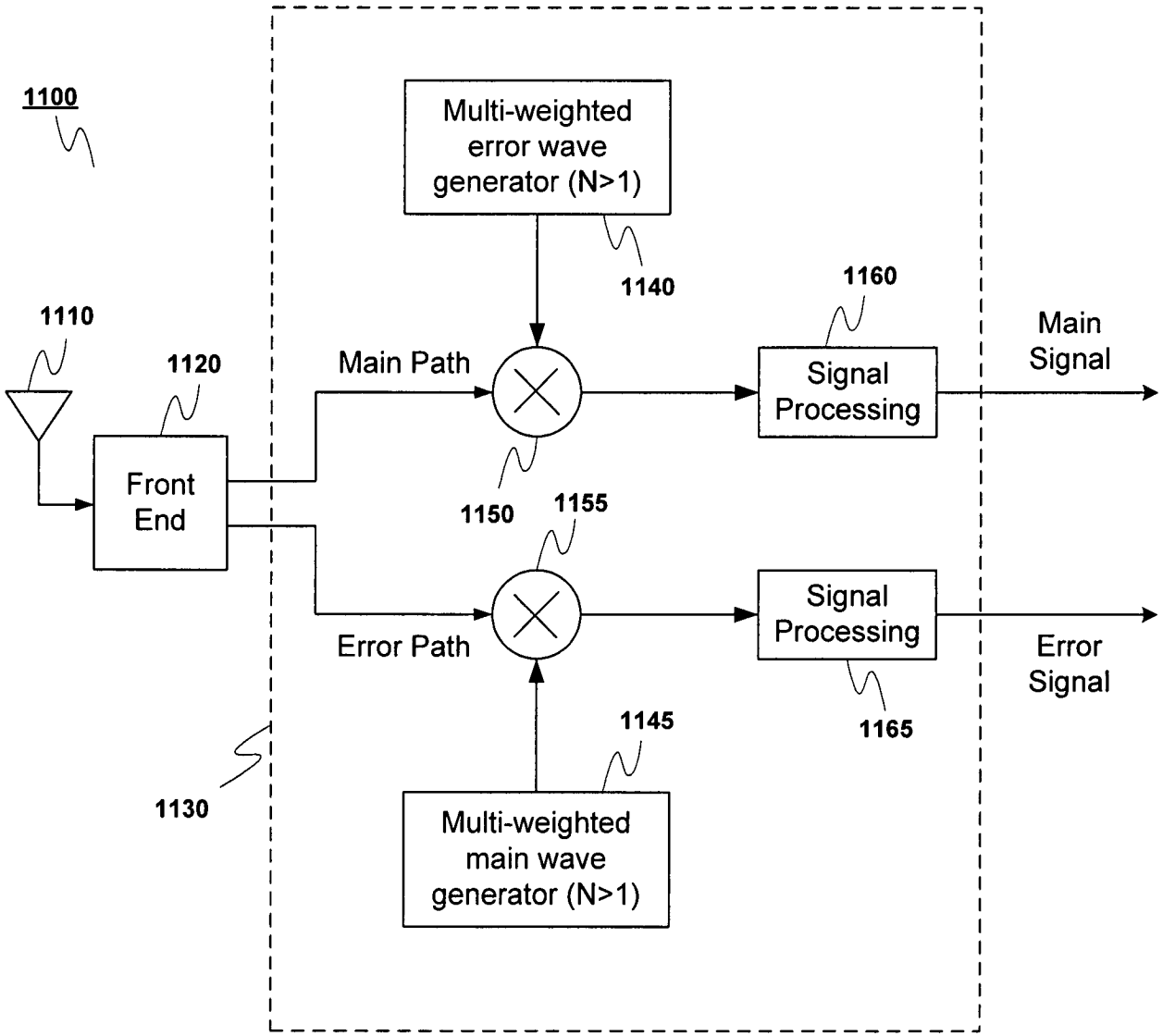
1100
Multi-weighted error wave generator (N>1)
1140
1160
1110
1120
Main Path
Signal Processing
Main Signal
Front End
1150
1155
Signal Processing
Error Path
Error Signal
1145
1165
1130
Multi-weighted main wave generator (N>1)

Fig. 11

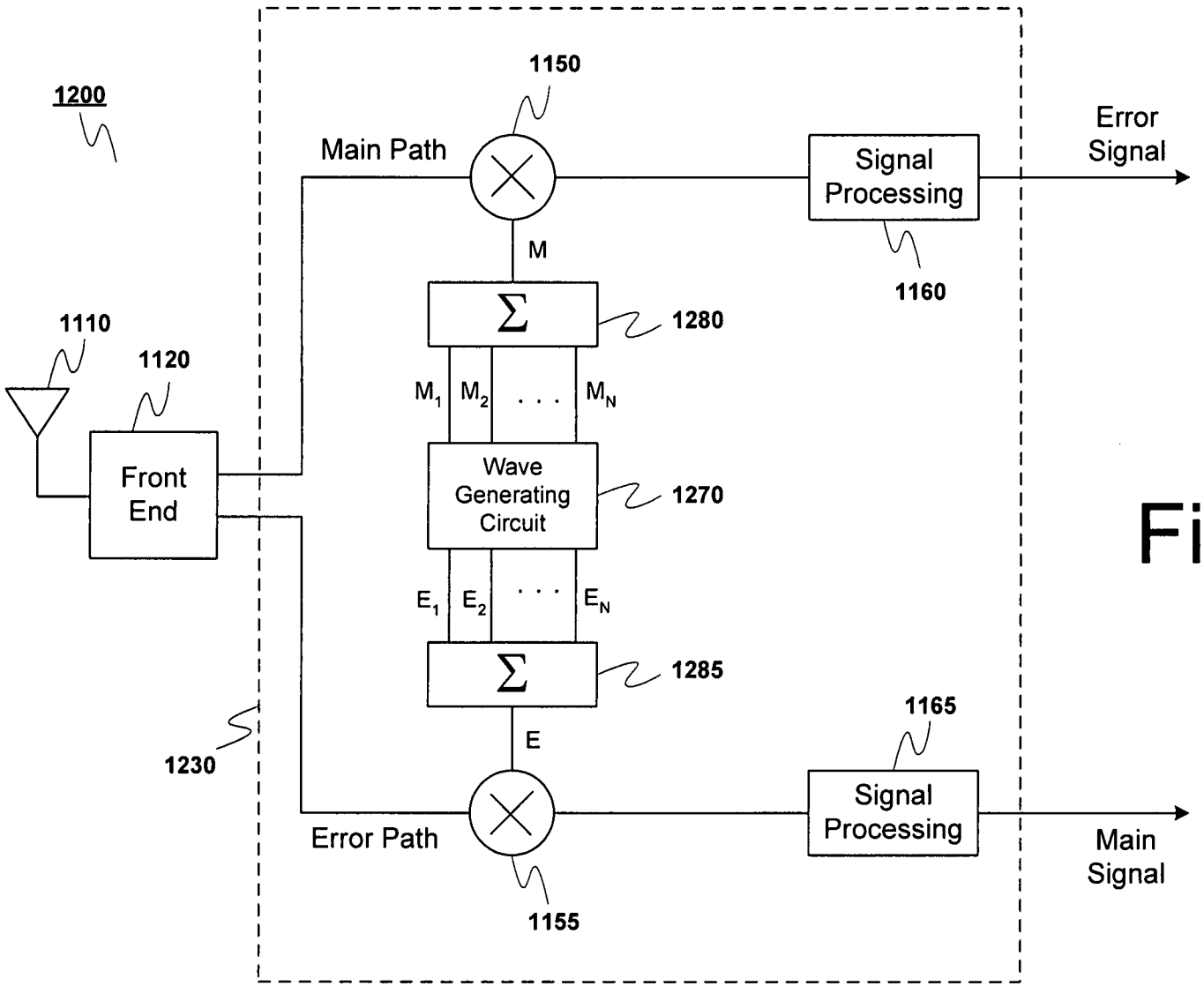
1200
1150
Main Path
Error Signal
Signal Processing
1160
M
1280
1110
1120
M_1 M_2 . . . M_N
Front End
Wave Generating Circuit
1270
E_1 E_2 . . . E_N
1285
1230
1165
E
Signal Processing
Error Path
Main Signal
1155

Fig. 12

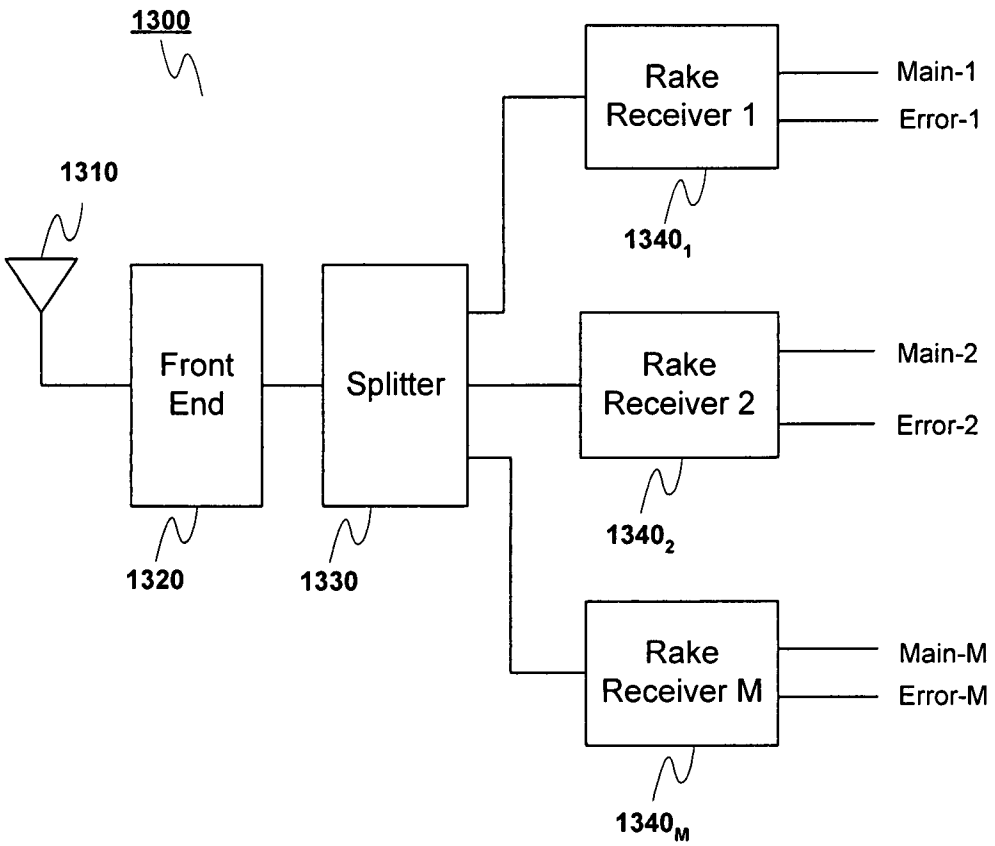
1300
1310
Front End
Splitter
Rake Receiver 1
Rake Receiver 2
Rake Receiver M
Main-1
Error-1
Main-2
Error-2
Main-M
Error-M
1320
1330
1340$_1$
1340$_2$
1340$_M$

Fig. 13

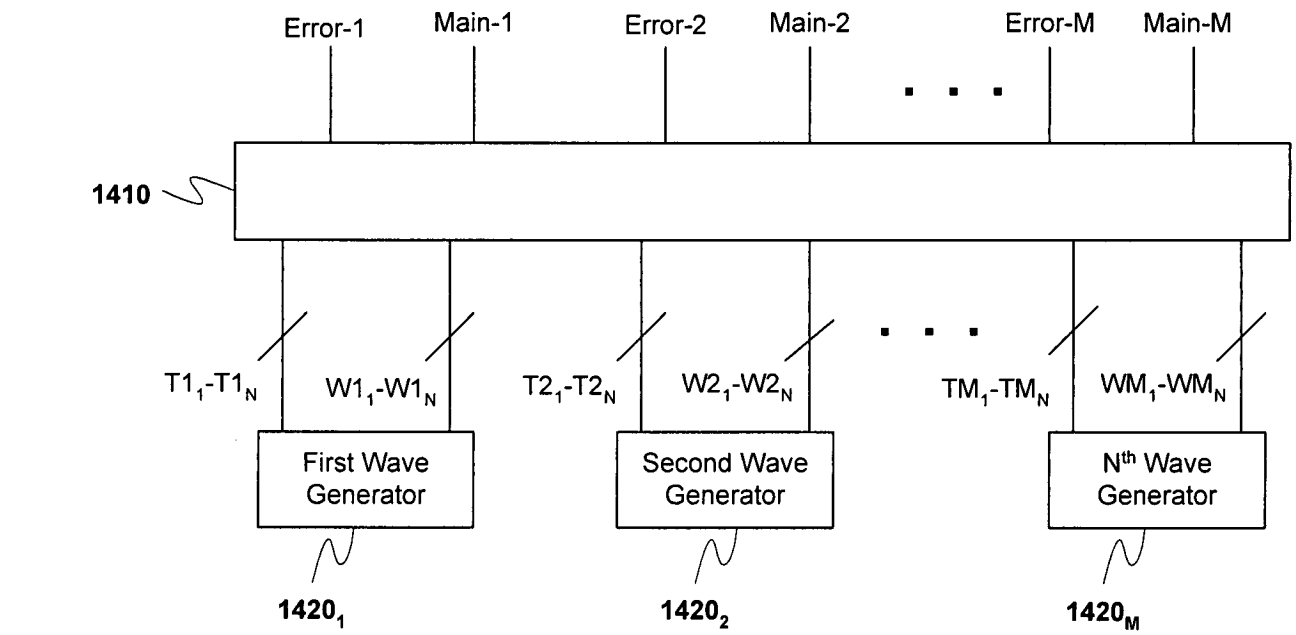
1400
Error-1
Main-1
Error-2
Main-2
Error-M
Main-M
1410
T1$_1$-T1$_N$
W1$_1$-W1$_N$
T2$_1$-T2$_N$
W2$_1$-W2$_N$
TM$_1$-TM$_N$
WM$_1$-WM$_N$
First Wave Generator
Second Wave Generator
Nth Wave Generator
1420$_1$
1420$_2$
1420$_M$

Fig. 14

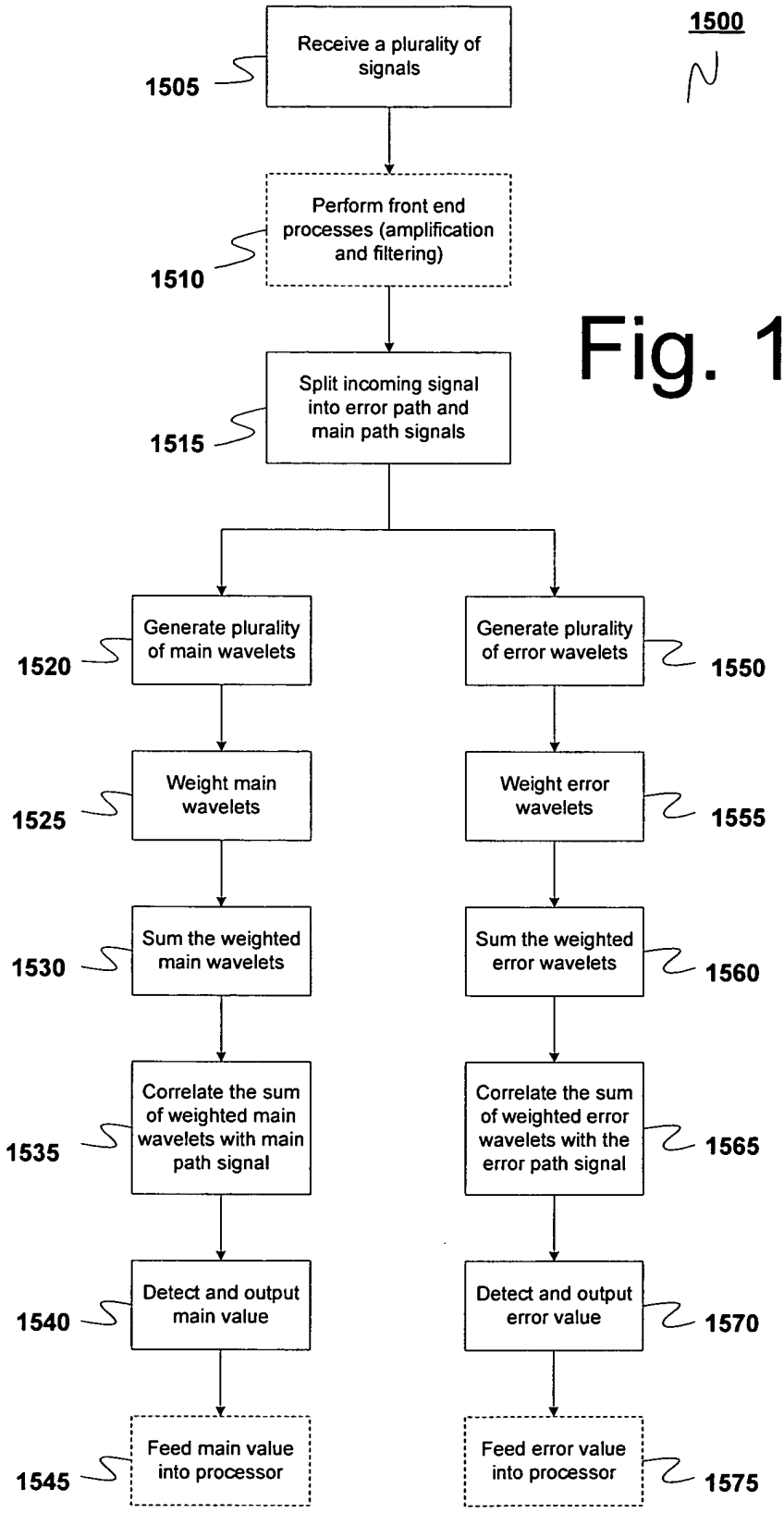
1500
Receive a plurality of signals
1505
Perform front end processes (amplification and filtering)
1510
Split incoming signal into error path and main path signals
1515
Generate plurality of main wavelets
1520
Weight main wavelets
1525
Sum the weighted main wavelets
1530
Correlate the sum of weighted main wavelets with main path signal
1535
Detect and output main value
1540
Feed main value into processor
1545
Generate plurality of error wavelets
1550
Weight error wavelets
1555
Sum the weighted error wavelets
1560
Correlate the sum of weighted error wavelets with the error path signal
1565
Detect and output error value
1570
Feed error value into processor
1575

Fig. 15